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09/586,191	06/02/2000	Adrian J. Isles	HDCA1003USO	6083

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EXAMINER
SHARON, AYAL I

ART UNIT	PAPER NUMBER
2123	6

DATE MAILED: 07/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/586,191	ISLES, ADRIAN J.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 0200* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. Claims 1-44 of U.S. Application 09/586,191 filed on 06/02/2000 are presented for examination.

Drawings

2. The drawings are objected to because Figures 2 and 3 are listed in the specification (p.6) as being flowcharts. Figures 4 and 5 are listed in the specification (p.6) as being "exemplar operations". The labels for Figs. 2 and 4, and Figs. 3 and 5, respectively, appear to have switched. A Fig.6 is listed in the specification (p.6), yet none has been provided. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. The prior art used for these rejections is as follows:

5. Weems, Charles C. Jr. "CmpSci 535 Notes from Lecture 9: Memory Hierarchy and Caching". © 1996. (Henceforth referred to as "**Weems**").

6. Bayoumi, M. et al. "A Look-Up Table VLSI Design Methodology for RNS Structures Used in DSP Applications." IEEE Transactions on Circuits and Systems. Vol. 34, Issue 6, June 1997. pp.604-616. (Henceforth referred to as "**Bayoumi**").

7. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

8. **Claims 1-22, and 29-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Weems.**

9. In regards to Claim 1, Weems teaches the following limitations:

> 1. A method for modeling a physical memory for use in an electronic design, the method comprising the steps of:
>
> modeling a memory write operation using a lookup table; and
> (Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")
>
> modeling a memory read operation using the lookup table.
> (Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write")

10. In regards to Claim 2, Weems teaches the following limitations:

> 2. The method of claim 1, wherein the step of modeling a memory write operation comprises the steps of:
>
> receiving a plurality of write address bits corresponding to a write address of the physical memory to which a plurality of write data bits are written by the electronic design;
> (Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")
>
> receiving the plurality of write data bits corresponding to write data

written to the physical memory at the write address; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

determining whether the lookup table comprises a first entry that contains the plurality of write address bits in an address field and a valid bit of the first entry is asserted.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

11. In regards to Claim 3, Weems teaches the following limitations:

3. The method of claim 2, wherein the step of modeling a memory write operation further comprises the step of:

writing the plurality of write data bits to a data field of the first entry if the first entry contains the plurality of write address bits in the address field and a valid bit of the first entry is asserted.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

12. In regards to Claim 4, Weems teaches the following limitations:

4. The method of claim 2, wherein the step of modeling a memory write operation further comprises the following steps if the first entry does not contain the plurality of write address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write address bits to an address field of the second entry;
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

13. In regards to Claim 5, Weems teaches the following limitations:

5. The method of claim 1, wherein the step of creating a memory

read operation comprises the steps of:

receiving a plurality of read address bits corresponding to a read address of the physical memory from which a plurality of read data bits are read by the electronic design; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises a first entry that contains the plurality of read address bits in an address field and a valid bit of the first entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

14. In regards to Claim 6, Weems teaches the following limitations:

6. The method of claim 5, wherein the step of creating a memory read operation further comprises the step of:

returning the plurality of read data bits from a data field of the first entry if the first entry contains the plurality of read address bits in the address field and a valid bit of the first entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

15. In regards to Claim 7, Weems teaches the following limitations:

7. The method of claim 5, wherein the step of creating a memory read operation further comprises the following steps if the first entry does not contain the plurality of read address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary data value to a data field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and
returning the arbitrary data value.

(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

16. In regards to Claim 8, Weems teaches the following limitations:

8. The method of claim 7, wherein the arbitrary data value represents an initial value of the plurality of read data bits after an initialization step.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

17. In regards to Claim 9, Weems teaches the following limitations:

9. The method of claim 1, wherein a number of entries in the lookup is limited by a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by the steps of:

computing a total number of memory operations that can be performed per clock cycle; and
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

multiplying the total number of memory operations that can be performed per clock cycle by the given number of clock cycles.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

18. In regards to Claim 10, Weems teaches the following limitations:

10. The method of claim 9, further comprising the steps of:
determining a number of memory read operations in a property; and

adding the number of memory read operations in a property to the total number of memory operations.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

19. In regards to Claim 11, Weems teaches the following limitations:

11. The method of claim 1, further comprising the step of:
initializing a plurality of bits in a data field of an entry of the lookup table to an initial value.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

20. In regards to Claim 12, Weems teaches the following limitations:

12. A method for modeling an uninterpreted combinational block of an electronic circuit design in a lookup table, the uninterpreted combinational block being represented by a combinational function having an argument, the method comprising the steps of:

initializing the lookup table;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving the argument;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises a first entry that contains the argument in an address field of the first entry and a valid bit of the first entry is asserted; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

returning a data value in a data field of the first entry if the first entry contains the argument and the valid bit of the first entry is asserted, the data value being associated with the argument.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

21. In regards to Claim 13, Weems teaches the following limitations:

13. The method of claim 12, further comprising the steps of writing the argument to an address field of a second entry having an unasserted valid bit, assigning an arbitrary data value to a data field of the second entry wherein the arbitrary data value is prospectively associated with the argument, asserting the valid bit of the second entry, and returning the arbitrary data value if the lookup table does not comprise a first entry that contains the argument in the address field of the first entry and the valid bit of the first entry is not asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

22. In regards to Claim 14, Weems teaches the following limitations:

14. A method for modeling a physical memory in an electronic circuit design, the method comprising the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

modeling a memory write operation in a memory model to represent a memory write operation in the physical memory; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the memory model comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

23. In regards to Claim 15, Weems teaches the following limitations:

15. The method of claim 14, wherein the plurality of write data bits are written to a data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

24. In regards to Claim 16, Weems teaches the following limitations:

16. The method of claim 14, further comprising the following steps if the entry does not contain the plurality of write address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

25. In regards to Claim 17, Weems teaches the following limitations:

17. The method of claim 14, further comprising the steps of:

receiving a plurality of read address bits corresponding to a read

address of the physical memory from which the electronic circuit design reads a plurality of read data bits;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

modeling a memory read operation in the memory model to represent a memory read operation in the physical memory; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the entry contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

26. In regards to Claim 18, Weems teaches the following limitations:

18. The method of claim 17, wherein the plurality of read data bits from a data field of the entry is returned if the entry contains the plurality of read address bits in the address field and the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

27. In regards to Claim 19, Weems teaches the following limitations:

19. The method of claim 17, further comprising the following steps if the entry does not contain the plurality of read address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and
returning the arbitrary value.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

28. In regards to Claim 20, Weems teaches the following limitations:

20. The method of claim 14, wherein the memory model comprises a lookup table.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

29. In regards to Claim 21, Weems teaches the following limitations:

21. The method of claim 20, wherein a total number of entries of the lookup table is greater than or substantially equal to a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by the steps of:

determining a number of read ports of the physical memory;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining a number of write ports of the physical memory;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

computing a total number of memory operations that can be performed per clock cycle; and
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

multiplying the total number of memory operations that can be performed per clock cycle with the given number of clock cycles.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

30. In regards to Claim 22, Weems teaches the following limitations:

22. The method of claim 21, further comprising the steps of:
determining a number of memory read operations in a property; and
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

adding the number of memory read operations in a property to the total number of memory operations.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

31. In regards to Claim 29, Weems teaches the following limitations:

29. A processor readable storage medium having processor readable code embodied on the processor readable storage medium, the processor readable code for programming a processor to perform a method for creating a memory model for use in modeling an electronic circuit design having a physical memory, the method comprising the steps of:

modeling a memory write operation using a lookup table; and

(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

modeling a memory read operation using the lookup table.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write")

32. In regards to Claim 30, Weems teaches the following limitations:

30. The processor readable storage medium of claim 29, wherein the step of modeling a memory write operation comprises the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which a plurality of write data bits are written by the electronic design;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

receiving the plurality of write data bits written to the physical memory at the write address;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

determining whether the lookup table comprises a first entry that contains the plurality of write address bits in an address field and a valid bit of the first entry is asserted; and
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the first entry if the first entry contains the plurality of write address bits in the address field and the valid bit of the first entry is asserted.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

33. In regards to Claim 31, Weems teaches the following limitations:

31. The processor readable storage medium of claim 30, wherein the step of modeling a memory write operation further comprises the following steps if the first entry does not contain the plurality of write address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write address bits to an address field of the

second entry;
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

34. In regards to Claim 32, Weems teaches the following limitations:

32. The processor readable storage medium of claim 29, wherein the step of creating a memory read operation comprises the steps of:

receiving a plurality of read address bits corresponding to a read address of the physical memory from which a plurality of read data bits are read by the electronic design;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises a first entry that contains the plurality of read address bits in an address field and a valid bit of the first entry is asserted; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

returning the plurality of read data bits from a data field of the first entry if the first entry contains the plurality of read address bits in the address field and the valid bit of the first entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

35. In regards to Claim 33, Weems teaches the following limitations:

33. The processor readable storage medium of claim 32, wherein the step of creating a memory read operation further comprises the following steps if the first entry does not contain the plurality of read address bits in the address field and the valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;

(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and
returning the arbitrary value.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

36. In regards to Claim 34, Weems teaches the following limitations:

34. An apparatus for creating a memory model for use in modeling an electronic design having a physical memory, the apparatus comprising:

an output device;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

a processor, in communication with the output device; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

a processor readable storage medium for storing code, the processor readable storage medium being in communication with the processor, the code capable of programming the processor to perform the steps of:
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits;

(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

modeling a memory write operation using a memory model;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

modeling a memory read operation using the memory model;
determining whether the memory model comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the entry contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

37. In regards to Claim 35, Weems teaches the following limitations:

35. The apparatus of claim 34, wherein the code capable of programming the processor performs the following steps if the entry does not contain the plurality of read address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and
returning the arbitrary value.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

38. In regards to Claim 36, Weems teaches the following limitations:

36. The apparatus of claim 34, wherein the code capable of programming the processor further comprises the step of:

returning the plurality of read data bits from a data field of the entry if the entry contains the plurality of read address bits in the address field and the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

39. In regards to Claim 37, Weems teaches the following limitations:

37. The apparatus of claim 34, wherein the code capable of programming the processor performs the following steps if the entry does not contain the plurality of write address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

40. In regards to Claim 38, Weems teaches the following limitations:

38. The apparatus of claim 34, wherein the code capable of programming the processor further comprises the step of:

writing the plurality of write data bits to a data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

41. In regards to Claim 39, Weems teaches the following limitations:

39. The apparatus of claim 34, wherein the memory model comprises a lookup table.

(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

42. In regards to Claim 40, Weems teaches the following limitations:

40. The apparatus of claim 39, wherein a total number of entries of the lookup table is greater than or substantially equal to a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by the steps of:

determining a number of read ports of the physical memory;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining a number of write ports of the physical memory;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

computing a total number of memory operations that can be performed by the electronic design per clock cycle; and
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

multiplying the total number of memory operations that can be performed per clock cycle by the given number of clock cycles.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

43. In regards to Claim 41, Weems teaches the following limitations:

41. The apparatus of claim 40, further comprising the steps of:

determining a number of memory read operations in a property, the property being a set of behaviors of the physical memory; and
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

adding the number of memory read operations in a property to the total number of memory operations.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

44. In regards to Claim 42, Weems teaches the following limitations:

42. An apparatus for creating a model of an uninterpreted combinational block of an electronic circuit design using a lookup table, the uninterpreted combinational block being represented by a combinational function having an argument, the apparatus comprising:

an output device;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

a processor, in communication with the output device; and

(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

a processor readable storage medium for storing code, the processor readable storage medium being in communication with the processor, the code capable of programming the processor to perform the steps of:
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving the argument;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises a first entry that contains the argument in an address field of the first entry and a valid bit of the first entry is asserted; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

returning a data value in a data field of the first entry if the first entry contains the argument and the valid bit of the first entry is asserted, the data value being associated with the argument.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

45. In regards to Claim 43, Weems teaches the following limitations:

43. The apparatus of claim 42, wherein the code capable of programming the processor further comprises the step of:
initializing the lookup table.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

46. In regards to Claim 44, Weems teaches the following limitations:

44. The apparatus of claim 42, wherein the code capable of programming the processor further comprises the steps of writing the argument to an address field of a second entry having an unasserted valid bit, assigning an arbitrary data value to a data field of the second entry wherein the arbitrary data value is prospectively associated with the argument, asserting the valid bit of the second entry, and returning the arbitrary data value if the lookup table does not comprise a first entry that contains the argument in the address field of the first entry and the valid bit of the first entry is not asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

47. Claim 23 is rejected under 35 U.S.C. 102(b) as being anticipated by Bayoumi.

48. In regards to Claim 23, Weems teaches the following limitations:

23. A method for modeling an electronic circuit design having a physical memory, the physical memory being represented by a lookup table, the method comprising the steps of:

creating the lookup table, the lookup table having a total number of entries that is greater than or substantially equal to an upper limit;
(Bayoumi, especially: pp.605-607, "III. RNS-Based Systems in the VLSI Medium", "IV. A Look-Up Table Layout Methodology")

creating a hardware description language description of the memory model and a plurality of components of the electronic circuit design;
(Bayoumi, especially: pp.605-607, "III. RNS-Based Systems in the VLSI Medium", "IV. A Look-Up Table Layout Methodology")

synthesizing a gate level description of the memory model and the plurality of components of the electronic circuit design;
(Bayoumi, especially: pp.605-607, "III. RNS-Based Systems in the VLSI Medium", "IV. A Look-Up Table Layout Methodology")

verifying operation of the electronic circuit design using a set of properties.
(Bayoumi, especially: pp.605-607, "III. RNS-Based Systems in the VLSI Medium", "IV. A Look-Up Table Layout Methodology")

Claim Rejections - 35 USC § 103

49. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

50. The prior art used for these rejections is as follows:

51. Weems, Charles C. Jr. "CmpSci 535 Notes from Lecture 9: Memory Hierarchy and Caching". © 1996. (Henceforth referred to as "**Weems**").

52. Bayoumi, M. et al. "A Look-Up Table VLSI Design Methodology for RNS Structures Used in DSP Applications." IEEE Transactions on Circuits and Systems. Vol. 34, Issue 6, June 1997. pp.604-616. (Henceforth referred to as "**Bayoumi**").

53. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

54. Claims 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bayoumi in view of Weems.

55. In regards to Claim 24, Bayoumi does not expressly teach the following limitations regarding the behavior of a lookout table. Weems, however, does teaches the following limitations:

24. The method of claim 23, wherein the step of creating the memory model comprises the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises an entry that contains

the plurality of read address bits in the address field and whether the valid bit of the entry is asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

returning the plurality of read data bits from a data field of the entry if the entry contains the plurality of read address bits in the address field and a valid bit of the entry is asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

writing the plurality of write data bits to the data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

Bayoumi teaches "selecting the most efficient layout" for "developing a lookout table" in VLSI (see Bayoumi Abstract).

Weems teaches the behavior of the finished "Basic Cache Structures" (see Weems, p.3) and metrics for caches on existing processors (see Weems, pp.9-10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Bayoumi with those of Weems, because doing so would make it easier to analyze the design produced by Bayoumi, and would also make it easier to compare that design to existing designs.

56. In regards to Claim 25, Weems teaches the following limitations:

25. The method of claim 24, further comprising the following steps if the entry does not contain the plurality of read address bits in the address

field and a valid bit of the entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and
returning the arbitrary value.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

57. In regards to Claim 26, Weems teaches the following limitations:

26. The method of claim 24, further comprising the following steps if the entry does not contain the plurality of write address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

writing the plurality of write address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

asserting the valid bit of the second entry.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

58. In regards to Claim 27, Weems teaches the following limitations:

27. The method of claim 23, wherein the upper limit represents a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by the steps of:

determining a total number of memory read ports in the physical memory;
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

determining a total number of memory write ports in the physical memory;
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

computing a total number of memory operations that can be performed per clock cycle;
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

multiplying the total number of memory operations that can be performed per clock cycle with the given number of clock cycles.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

59. In regards to Claim 28, Weems teaches the following limitations:

28. The method of claim 27, further comprising the steps of:

determining a number of memory read operations performed in the set of properties; and
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

adding the number of memory read operations performed in the set of properties to the total number of memory operations.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

Conclusion

60. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

61. Cunningham et al., U.S. Patent 5,555,199.

62. MacInnis et al., U.S. Patent 6,380,945.

63. Chang, Y. et al. "Cache Memory Protocols" Wiley Encyclopedia of Electrical and Electronics Engineering Online. Article Online Posting Date: Dec. 27, 1999.

64. Patten, W.N. et al. "A Minimum Time Seek Controller for a Disk Drive." IEEE Transactions on Magnetics. Vol.31, Issue 3, May 1995. pp.2380-2387.

65. Grochowski, E. et al. "Issues in the Implementation of the i486 Cache and Bus." 1989 IEEE Int'l Conf. on Computer Design. (ICCD '89). Oct. 4, 1989. pp.193-198.

66. Cong, J. et al. "FlowMap: An Optimal Technology Mapping Algorithm for Delay Optimization in Lookup-Table Based FPGA Designs." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Vol. 13, Issue 1, Jan.1994. pp.1-12.

67. Parhami, B. et al. "Optimal Table Lookup Schemes for VLSI Implementation of Input/Output Conversations and Other Residue Number Operations." [Workshop on] VLSI Signal Processing, VII, 1994. Oct. 28, 1994. pp.470-481.

68. Zukowski, C. et al. "Putting Routing Tables in Silicon", IEEE Network. Vol.6, Issue 1, Jan. 1992. pp.42-50.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

The fax phone numbers for the organization where this application or proceeding is assigned are:

Official communications:	(703) 746-7239
Non-Official / Draft communications	(703) 746-7240
After Final communications	(703) 746-7238

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is:

(703) 305-3900.

Ayal I. Sharon

Art Unit 2123

June 29, 2003

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PRIMARY EXAMINER